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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/919,797

08/02/2001

Hirotooshi Kubo

2001-1101

4860

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7590

11/20/2002

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WASHINGTON, DC 20006-1021

EXAMINER

VOCKRODT, JEFF B

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/919,797

Applicant(s)

KUBO, HIROTOSHI

Examiner

Jeff Vockrodt

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 02 August 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

This office action is in response to the application papers filed on August 2, 2001.

Claims 1-8 are pending.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 1-5 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 4,997,775 ("Cook").**

Claim 1 reads on Cook as follows: A method of manufacturing a semiconductor device, comprising: forming a collector layer (16; Fig. 6) of a first conductivity type (N); forming a base region (66,68) of a second conductivity type (P) formed on a top surface of said collector layer (16) of said first conductivity type (N), said first conductivity type (N) being opposite said second conductivity type (P), said base region (66, 68) being formed as a single region (the base is formed contiguously) having uniform depth thereof (the lower portion of the base 66, 68 is a uniform depth as measured from the substrate surface), forming a groove (62) in a top surface of said base region (66, 68) at a portion thereof; and forming an emitter region (74; Fig. 8) of said first conductivity type (N) in said base region (66, 68) at a bottom surface of said groove (Fig. 8).

Claim 2. A method of manufacturing a semiconductor device according to claim 1, wherein said base region (66, 68) on said top surface of said collector layer is formed by using an epitaxial growth technology (the entire structure is formed by using an epitaxial growth technology; col. 3, ll. 14-20).

Claim 3. A method of manufacturing a semiconductor device according to claim 1, wherein said base region (66, 68) is formed on said top surface of said collector layer (66, 68) by a diffusion of impurities at a prescribed diffusion depth (col. 5, ll. 9-24).

Claim 4. A method of manufacturing a semiconductor device according to claim 1, wherein said base region (66, 68) has a flat bottom surface beneath said emitter region (74) and beneath a base electrode (52D; Fig. 8)).

Claim 5. A method of manufacturing a semiconductor device according to claim 1, further comprising: forming spacers (66B) on sidewalls in said groove (62); forming a diffusion source film (71) in said bottom surface of said groove to be embedded therein between said spacers (66B); and forming said emitter region (74) of said first conductivity type (N) formed in said top surface of said base region (66, 68) at a bottom of said diffusion source film (74) between said spacers (66B).

Claim 8. A method of manufacturing a semiconductor device according to claim 1, wherein said diffusion source film (71) is a polycrystalline silicon layer having impurities for emitter diffusion (74) (col. 5, ll. 45-51).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cook in view of U.S. Pat. No. 4,731,341 ("Kawakatsu").**

Claim 6 differs from Cook by forming an emitter electrode on the surface of the diffusion source film. Claim 7 differs from Cook by forming the base and emitter electrodes of aluminum.

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Cook merely teaches a doped polysilicon diffusion source film (71) that serves as the emitter electrode.

Kawakatsu teaches forming a bipolar transistor utilizing an arsenic doped polysilicon emitter contact layer 116 from which the emitter dopants are diffused and an aluminum emitter electrode 116. (Kawakatsu, col. 4, ll. 50-60).

Cook and Kawakatsu are analogous art. They are within the field of bipolar transistors and particularly teach forming diffused emitters.

Further forming an aluminum electrode onto the emitter electrode (71) of Cook would have been obvious to one of ordinary skill in the art at the time of the invention. A person having ordinary skill in the art would have been motivated to form an aluminum electrode in addition to the emitter electrode of Cook to facilitate improved electrical contact to the emitter as suggested by Kawakatsu.

### ***Conclusion***

Any inquiry concerning communications from the examiner should be directed to Jeff Vockrodt at (703) 306-9144 who can be reached on weekdays from 9:30 am to 5:00 pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (703) 308-4905.

The fax numbers for this Group are (703) 305-3432, (703) 308-7722, (703) 305-3431, and (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist at (703) 308-0956.

November 12, 2002

J. Vockrodt



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